N-Channel Depletion-Mode Vertical DMOS FET

Features

- High input impedance
- Low input capacitance
- Fast switching speeds
- Low on-resistance
- Free from secondary breakdown
- Low input and output leakages

Applications

- Normally-on switches
- Battery operated systems
- Converters
- Linear amplifiers
- Constant current sources
- Telecom

General Description

This low threshold, depletion-mode (normally-on) transistor utilizes an advanced vertical DMOS structure and Supertex's well proven silicon-gate manufacturing process. This combination produces a device with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, this device is free from thermal runaway and thermally-induced secondary breakdown.

Supertex's vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where a very low threshold voltage, high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Ordering Information

Part Number	Package Option	Packing
DN1509K1-G	5-Lead SOT-23	2500/Reel
DN1509N8-G	TO-243AA (SOT-89)	2000/Reel

-G denotes a lead (Pb)-free / RoHS compliant package

Product Summary

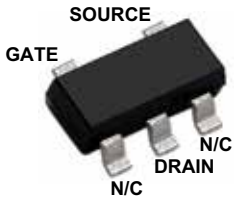
BV_{DSX}/BV_{DGX} (V)	$R_{DS(ON)}$ (max) (Ω)	I_{DSS} (min) (mA)
90	6.0	300

Absolute Maximum Ratings

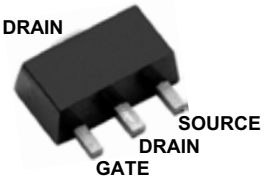
Parameter	Value
Drain-to-source voltage	BV_{DSX}
Drain-to-gate voltage	BV_{DGX}
Gate-to-source voltage	±20V
Operating and storage temperature	-55°C to +150°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

Pin Configuration



5-Lead SOT-23



TO-243AA (SOT-89)

Typical Thermal Resistance

Package	θ_{ja}
5-Lead SOT-23	253°C/W
TO-243AA (SOT-89)	78°C/W†

Notes:

† Mounted on FR4 board, 25mm x 25mm x 1.57mm.

Product Marking

W = Code for week sealed
_____ = "Green" Packaging

Package may or may not include the following marks: Si or ⏚

5-Lead SOT-23

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TO-243AA (SOT-89)

Thermal Characteristics

Package	I_D† (continuous) (mA)	I_D (pulsed) (mA)	Power Dissipation @T_A = 25°C (W)	I_{DR}† (mA)	I_{DRM} (mA)
5-Lead SOT-23	200	500	0.49	200	500
TO-243AA	360	500	1.6‡	360	500

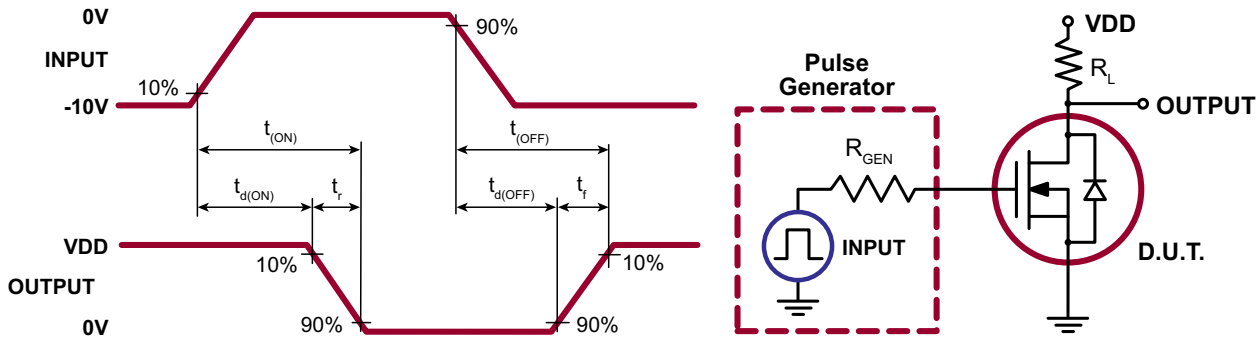
Notes:
† I_D (continuous) is limited by max rated T_j.
‡ Mounted on FR4 board, 25mm x 25mm x 1.57mm.

Electrical Characteristics *(T_j = 25°C unless otherwise specified)*

Sym	Parameter	Min	Typ	Max	Units	Conditions
BV_{DSX}	Drain-to-source breakdown voltage	90	-	-	V	V_{GS} = -5V, I_D = 1.0µA
$V_{GS(OFF)}$	Gate-to-source off voltage	-1.8	-	-3.5	V	I_D = 10µA
$\Delta V_{GS(OFF)}$	$V_{GS(OFF)}$ change with temperature	-	-	-4.5	mV/°C	V_{DS} = 15V, I_D = 10µA
I_{GSS}	Gate body leakage	-	-	100	nA	V_{GS} = ±20V, V_{DS} = 0V
$I_{D(OFF)}$	Drain-to-source leakage current	-	-	1.0	µA	V_{DS} = Max rating, V_{GS} = -5.0V
		-	-	1.0	mA	V_{DS} = 0.8 Max Rating, V_{GS} = -5.0V, T_A = 125°C
I_{DSS}	Saturated drain-to-source current	300	540	-	mA	V_{GS} = 0V, V_{DS} = 25V
$R_{DS(ON)}$	Static drain-to-source on-state resistance	-	3.2	6.0	Ω	V_{GS} = 0V, I_D = 200mA
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with temperature	-	-	1.1	%/°C	V_{GS} = 0V, I_D = 200mA
G_{FS}	Forward transconductance	200	-	-	mmho	V_{DS} = 10V, I_D = 200mA
C_{ISS}	Input capacitance	-	70	150	pF	V_{GS} = -10V, V_{DS} = 25V, f = 1MHz
C_{OSS}	Common source output capacitance	-	20	40		
C_{RSS}	Reverse transfer capacitance	-	6.0	15		
$t_{d(ON)}$	Turn-on delay time	-	12	30	ns	V_{DD} = 25V, I_D = 100mA, R_{GEN} = 25Ω
t_r	Rise time	-	16	45		
$t_{d(OFF)}$	Turn-offF delay time	-	15	45		
t_f	Fall time	-	25	60		
V_{SD}	Diode forward voltage drop	-	-	1.8	V	V_{GS} = 0V, I_{SD} = 500mA
t_{rr}	Reverse recovery time	-	400	-	ns	V_{GS} = 0V, I_{SD} = 500mA

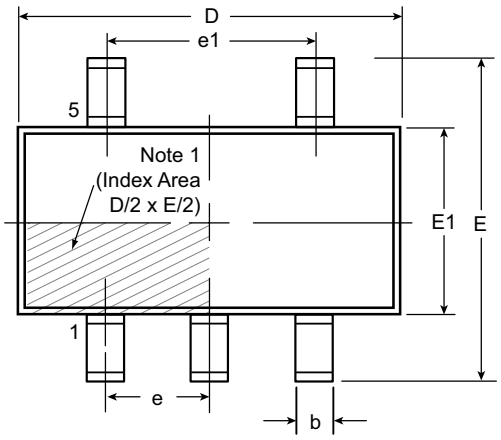
Notes:
1. *All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)*
2. *All A.C. parameters sample tested.*

Switching Waveforms and Test Circuit

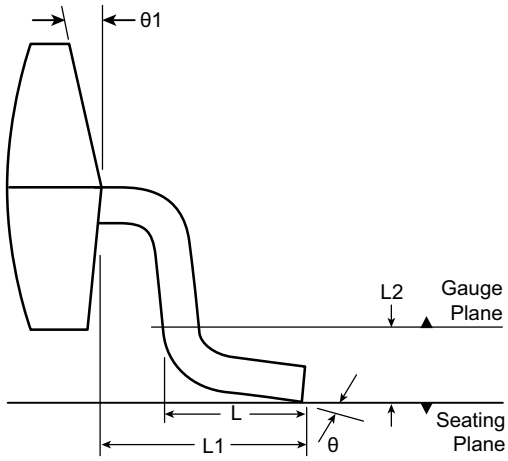


5-Lead SOT-23 Package Outline (K1)

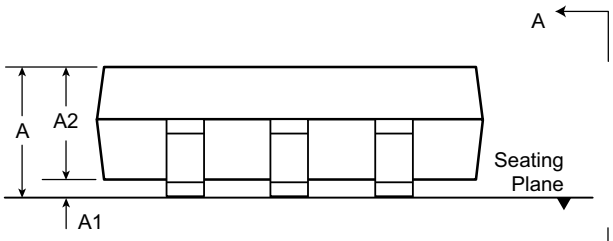
2.90x1.60mm body, 1.45mm height (max), 0.95mm pitch



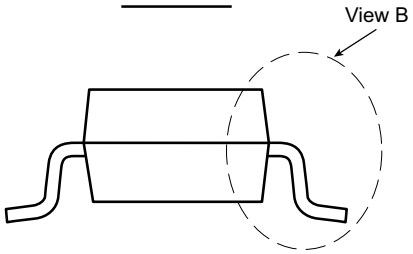
Top View



View B



Side View



View A - A

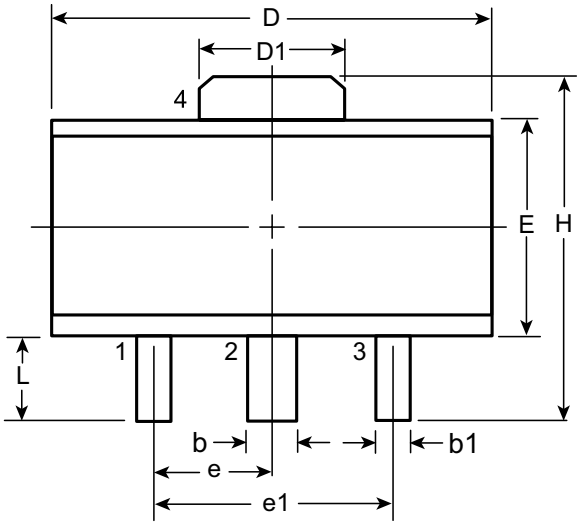
Note:

1. *A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*

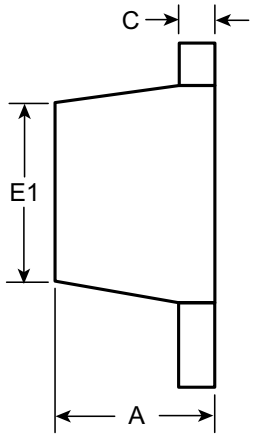
Symbol		A	A1	A2	b	D	E	E1	e	e1	L	L1	L2	θ	θ1
Dimension (mm)	MIN	0.90*	0.00	0.90	0.30	2.75*	2.60*	1.45*	0.95 BSC	1.90 BSC	0.30	0.60 REF	0.25 BSC	0°	5°
	NOM	-	-	1.15	-	2.90	2.80	1.60			0.45			4°	10°
	MAX	1.45	0.15	1.30	0.50	3.05*	3.00*	1.75*			0.60			8°	15°

JEDEC Registration MO-178, Variation AA, Issue C, Feb. 2000.
** This dimension is not specified in the JEDEC drawing.*
Drawings not to scale.
***Supertex Doc. #:** DSPD-5SOT23K1, Version A041309.*

3-Lead TO-243AA (SOT-89) Package Outline (N8)



Top View



Side View

Symbol		A	b	b1	C	D	D1	E	E1	e	e1	H	L
Dimensions (mm)	MIN	1.40	0.44	0.36	0.35	4.40	1.62	2.29	2.00†	1.50 BSC	3.00 BSC	3.94	0.73†
	NOM	-	-	-	-	-	-	-	-			-	-
	MAX	1.60	0.56	0.48	0.44	4.60	1.83	2.60	2.29			4.25	1.20

JEDEC Registration TO-243, Variation AA, Issue C, July 1986.
† *This dimension differs from the JEDEC drawing*
Drawings not to scale.
Supertex Doc. #: *DSPD-3TO243AAN8, Version F111010.*

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to http://www.supertex.com/packaging.html.)

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